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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,320	12/02/2003	Kwan-Yong Lim	P69335US0	5389

7590 09/10/2004

JACOBSON, PRICE, HOLMAN & STERN
PROFESSIONAL LIMITED LIABILITY COMPANY
400 Seventh Street, N.W.
Washington, DC 20004

EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,320	LIM ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanimoto et al. (US Patent 6392270) in view of Henderson (US Patent 4149307).

4. Tanimoto et al. teach a method for fabricating a gate electrode of a semiconductor device, comprising the steps of:

forming a gate insulation layer (103) on a substrate (fig. 5A);

forming a gate layer structure containing at least a metal layer (110) on the gate insulation layer;

forming a hard mask silicon oxide layer (111) on the gate layer structure;

forming a hard mask nitride layer (201) on the hard mask oxide layer;

patterning the hard mask oxide layer and the hard mask nitride layer as a double hard mask for forming the gate electrode (fig. 5B); and

forming the gate electrode by etching the gate layer structure with use of the double hard mask as an etch mask (fig. 5C). Wherein the gate layer structure is a structure selected from a stack structure of a metal layer, a diffusion barrier layer and a polysilicon layer, a stack structure of a silicide layer and a polysilicon layer, a stack structure of a metal layer, a diffusion barrier layer and a polysilicon-germanium layer and a single metal structure containing only a metal layer (col. 5 lines 32 – 36, & col. 6 lines 19 – 26).

5. Tanimoto et al. lack forming a hard mask oxide layer on the gate layer structure at a temperature lower than an oxidation temperature of the metal layer.

6. However, Henderson teaches forming a hard mask oxide layer on the gate layer structure at a temperature lower than an oxidation temperature of the metal layer (col. 3 line 57 – col. 4 line 2) to prevent oxidation of the gate material.

7. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate the teachings of Henderson into the Tanimoto et al. reference to prevent oxidation of the gate material.

8. Claims 1, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uehara et al. (US Patent 6573132) in view of Henderson (US Patent 4149307).

9. Uehara et al teach a method for fabricating a gate electrode of a semiconductor device, comprising the steps of:

forming a gate insulation layer (3) on a substrate (fig. 2B);

forming a gate layer structure (4, 5) containing at least a metal layer (5) on the gate insulation layer;

forming a composite hard mask (16/31) oxide layer and nitride layer on the gate layer structure with the oxide layer adjacent the gate layer (col. col. 9 lines 47 – 51);

patterning the hard mask oxide layer and the hard mask nitride layer as a double hard mask for forming the gate electrode, and forming the gate electrode by etching the gate layer structure with use of the double hard mask as an etch mask (fig. 2C).

10. Uehara et al. lack forming a hard mask oxide layer on the gate layer structure at a temperature lower than an oxidation temperature of the metal layer.

11. However, Henderson teaches forming a hard mask oxide layer on the gate layer structure at a temperature lower than an oxidation temperature of the metal layer (col. 3 line 57 – col. 4 line 2) to prevent oxidation of the gate material.

12. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate the teachings of Henderson into the Uehara et al. reference to prevent oxidation of the gate material.

13. Claims 2, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanimoto et al. (US Patent 6392270) in view of Henderson (US Patent 4149307), and further in view of Gambino et al. (US Patent 6689650).

14. The Henderson/Tanimoto et al. reference teaches the features previously outlined, but lacks ALD deposition of the of the hard mask oxide, and to a thickness of 10 – 1000 angstroms.

15. However, Gambino et al. teach ALD deposition of the of the hard mask oxide, and to a thickness of 10 – 1000 angstroms (col. lines 15 – 26).

16. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate the teachings of Gambino et al. into the Henderson/Tanimoto et al. reference as an etch stop.

17. Claims 3, 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uehara et al. (US Patent 6573132) in view of Henderson (US Patent 4149307), and further in view of Park et al. (USPAP 2002/0086507).

18. The Henderson/Uehara et al. reference teaches the features previously outlined, but lacks a hard mask silicon oxide layer of thickness of 10 – 1000 angstroms, and annealing the hard mask oxide layer in an atmosphere of nitrogen, hydrogen, or both for 10 sec – 30 minutes at a temperature range of 400 – 1000 degrees C.

19. However, Park et al. teach a hard mask silicon oxide layer of thickness of 10 – 1000 angstroms (paragraph 28), annealing the hard mask oxide layer of high dielectric material in an atmosphere of nitrogen, hydrogen, or combination thereof for 10 sec – 30 minutes, and further subjected to UV-ozone for removing impurity (paragraph 23).

20. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate the teachings of Park et al. into the Henderson/Uehara et al. reference to avoid poisoning the gate material.

21. Claims 8 – 15 are allowable, because prior art does not teach a composite hard mask comprising a nitride, a conductive layer, and an oxide layer adjacent a metal gate electrode of a gate stack for etching the gate stack.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2825

IA

September 1, 2004

C. Everhart
CARIDAD EVERHART
PRIMARY EXAMINER